

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Currently amended) A method for latching and amplifying a
2 capacitively coupled inter-chip communication signal, comprising:
3 receiving an input signal on a capacitive receiver pad from a capacitive
4 transmitter pad;
5 feeding the input signal through an inverter to produce an output signal;
6 feeding the output signal through a weakened inverter to produce a
7 feedback signal; and
8 feeding the feedback signal back into an input of the inverter so as to form
9 a latch for the input signal between the inverter and the weakened inverter; and
10 wherein the weakened inverter is biased to produce the feedback signal
11 that swings between a high bias voltage, V_H , and a low bias voltage, V_L ;
12 adjusting an RC time constant for the feedback signal so that the time
13 constant for the feedback signal is significantly larger than the time constant for
14 the transmitted signal from the capacitive transmitter pad, thereby ensuring that
15 the feedback signal does not mask transitions of the transmitted signal;
16 wherein V_H is slightly higher than a switching threshold of the inverter, and
17 V_L is slightly lower than the switching threshold of the inverter, whereby the
18 feedback signal causes the input signal to reside within a narrow voltage range
19 near the switching threshold of the inverter, thereby making the inverter sensitive
20 to small transitions in the input signal received on the capacitive receiver pad.

1 2. (Original) The method of claim 1, further comprising amplifying an
2 output of the inverter through an amplification stage to produce an amplified
3 output signal.

1 3. (Original) The method of claim 2, further comprising establishing the
2 high bias voltage, V_H , with a high bias voltage generator and establishing the low
3 bias voltage, V_L , with a low bias voltage generator.

1 4. (Original) The method of claim 3,
2 wherein the high bias voltage generator includes a mechanism for
3 adjusting the high bias voltage, V_H ; and
4 wherein the low bias voltage generator includes a mechanism for adjusting
5 the low bias voltage, V_L .

1 5. (Original) The method of claim 4, further comprising adjusting the high
2 bias voltage generator and the low bias voltage generator to provide a specified
3 sensitivity to transitions of the input signal.

1 6. (Original) The method of claim 4, further comprising adjusting the high
2 bias voltage generator and the low bias voltage generator to provide a specified
3 noise immunity to noise associated with the input signal.

1 7 (Canceled).

1 8. (Currently amended) An apparatus for latching and amplifying a
2 capacitively coupled inter-chip communication signal, comprising:
3 a receiving mechanism configured to receive an input signal on a
4 | capacitive receiver pad from a capacitive transmitter pad; and

5 a latching mechanism configured to feed the input signal through an
6 inverter to produce an output signal; and
7 an adjusting mechanism configured to adjust an RC time constant for the
8 feedback signal so that the time constant for the feedback signal is significantly
9 larger than the time constant for the transmitted signal from the capacitive
10 transmitter pad, thereby ensuring that the feedback signal does not mask
11 transitions of the transmitted signal;
12 wherein the latching mechanism is further configured to feed the output
13 signal through a weakened inverter to produce a feedback signal; and
14 wherein the latching mechanism is further configured to feed the feedback
15 signal back into an input of the inverter so as to form a latch for the input signal
16 between the inverter and the weakened inverter;
17 wherein the weakened inverter is biased to produce the feedback signal
18 that swings between a high bias voltage, V_H , and a low bias voltage, V_L ;
19 wherein V_H is slightly higher than a switching threshold of the inverter, and
20 V_L is slightly lower than the switching threshold of the inverter, whereby the
21 feedback signal causes the input signal to reside within a narrow voltage range
22 near the switching threshold of the inverter, thereby making the inverter sensitive
23 to small transitions in the input signal received on the capacitive receiver pad.

1 9. (Original) The apparatus of claim 8, further comprising an amplifying
2 mechanism configured to amplify an output of the inverter through an
3 amplification stage to produce an amplified output signal.

1 10. (Original) The apparatus of claim 9, further comprising a biasing
2 mechanism configured to establishing the high bias voltage, V_H , with a high bias
3 voltage generator and establishing the low bias voltage, V_L , with a low bias
4 voltage generator.

1 11. (Original) The apparatus of claim 10,
2 wherein the high bias voltage generator includes a mechanism for
3 adjusting the high bias voltage, V_H ; and
4 wherein the low bias voltage generator includes a mechanism for the low
5 bias voltage, V_L .

1 12. (Original) The apparatus of claim 11, further comprising an adjusting
2 mechanism configured to adjust the high bias voltage generator and the low bias
3 voltage generator to provide a specified sensitivity to transitions of the input
4 signal.

1 13. (Original) The apparatus of claim 11, further comprising an adjusting
2 mechanism configured to adjust the high bias voltage generator and the low bias
3 voltage generator to provide a specified noise immunity to noise associated with
4 the input signal.

1 14 (Canceled).

1 15. (Currently amended) A means for latching and amplifying a
2 capacitively coupled inter-chip communication signal, comprising:
3 a receiving means for receiving an input signal on a capacitive receiver
4 pad from a capacitive transmitter pad; ~~and~~
5 a latching means configured to feed the input signal through an inverter to
6 produce an output signal; and
7 an adjusting means for adjusting an RC time constant for the feedback
8 signal so that the time constant for the feedback signal is significantly larger than
9 the time constant for the transmitted signal from the capacitive transmitter pad.

10 | thereby ensuring that the feedback signal does not mask transitions of the
11 | transmitted signal;

12 | wherein the latching means is further configured to feed the output signal
13 | through a weakened inverter to produce a feedback signal; and

14 | wherein the latching means is further configured to feed the feedback
15 | signal back into an input of the inverter so as to form a latch for the input signal
16 | between the inverter and the weakened inverter;

17 | wherein the weakened inverter is biased to produce the feedback signal
18 | that swings between a high bias voltage, V_H , and a low bias voltage, V_L ;

19 | wherein V_H is slightly higher than a switching threshold of the inverter, and
20 | V_L is slightly lower than the switching threshold of the inverter, whereby the
21 | feedback signal causes the input signal to reside within a narrow voltage range
22 | near the switching threshold of the inverter, thereby making the inverter sensitive
23 | to small transitions in the input signal received on the capacitive receiver pad.

1 16. (Original) The means of claim 15, further comprising an amplifying
2 | means for amplifying an output of the inverter through an amplification stage to
3 | produce an amplified output signal.

1 17. (Original) The means of claim 16, further comprising a biasing means
2 | for establishing the high bias voltage, V_H , with a high bias voltage generator and
3 | for establishing the low bias voltage, V_L , with a low bias voltage generator.

1 18. (Original) The means of claim 17,
2 | wherein the high bias voltage generator includes a mechanism for
3 | adjusting the high bias voltage, V_H ; and
4 | wherein the low bias voltage generator includes a mechanism for the low
5 | bias voltage, V_L .

1 19. (Original) The means of claim 18, further comprising an adjusting
2 means for adjusting the high bias voltage generator and the low bias voltage
3 generator to provide a specified sensitivity to transitions of the input signal.

1 20. (Original) The means of claim 18, further comprising an adjusting
2 means for adjusting the high bias voltage generator and the low bias voltage
3 generator to provide a specified noise immunity to noise associated with the input
4 signal.

1 21. (Canceled).